REMARKS

Claims 4-9, 11, and 13 are presently pending in the application. Claim 14 was canceled. Reconsideration and allowance of all claims are respectfully requested in view of the following remarks.

The Information Disclosure Statement (IDS) submitted November 7, 2002, has apparently not yet been considered by the Examiner. The Examiner is respectfully requested to consider the IDS and return an initialed PTO-1449 form to the Applicants with the next Office Action.

The Examiner has rejected Claim 4 due to an informality. Claim 4 has been amended to obviate any informality noted by the Examiner.

The Examiner has rejected Claims 4, 9 and 14 under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,281,552 to Kawasaki et al. The Examiner has also rejected Claims 5-7 and 11 under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. The Examiner has rejected Claim 13 also under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. in view of U.S. Patent No. 6,420,758 to Nakajima.

However, the Examiner has found Claim 8 allowable if rewritten into independent form including all of the limitations of the base claim including any intervening claims. Claim 8 has been rewritten into independent form which should result in its immediate allowance.

Claim 14 has been canceled. However, for the following reasons, the prior art rejections are respectfully traversed.

The Applicants respectfully submit that Kawasaki et al. do not teach or suggest a method of making a bottom-gate thin film transistor including the steps of: forming a laminate on the gate insulating film, including: forming a precursor film for an active layer; and forming a protective insulating film on the precursor film without using an etching process, the protective insulating film having a thickness of 100 nm or less; implanting a dopant when forming one of an LDD region and a source-drain region of the

precursor film for the active layer through the protective insulating film without etching the protective insulating film; and activating the implanted dopant so that a non-doped portion comprises the active layer, as recited in amended Claim 4.

Rather, Kawasaki et al. disclose forming a gate insulating film 105, then forming an amorphous silicon film that is crystallized to a crystalline silicon film 106, doping a region of the crystalline silicon film 106 by: depositing a silicon oxide or silicon nitride film on the crystalline silicon film 106, forming a photoresist film, exposing the photoresist film to light, and using gate electrodes 102 and 104 as masks to etch and remove portions to form first spacer films 107-109.

Thereafter, Kawasaki et al. disclose forming a second spacer film 110, doping the crystalline silicon film 106 through the second spacer film 110, forming impurity regions for the source region or drain region, removing the first and second spacer films and adding a protective insulating film 150 that forms part of an interlayer insulating film, and performing a heat treatment to activate the impurity elements.

However, contrary to the Examiner's assertions, the steps in Kawasaki et al. are completely different from that of the present invention.

First, Kawasaki et al. disclose, forming the first spacers 107-109 which are disposed on the crystalline silicon film 106, by depositing a silicon oxide or silicon nitride film on the crystalline silicon film 106, forming the photoresist film, then etching the photoresist film to form the spacers 107-109.

However, in the present invention, the protective insulating film 8 is formed on the precursor (i.e., polysilicon) film 7 without etching the protective insulating film, but rather, by a thermal CVD or plasma CVD process etc. Thereafter, the polysilicon film 7 is implanted with a dopant through the protective insulating film 8 without etching when forming the LDD region or the source-drain region.

However in Kawasaki et al., the LDD region or source-drain region is formed after the crystalline silicon film 106 is doped with an impurity element for imparting N type, then etched, doped again for N

type by ion doping through spacers 107-109 and 110 without etching, then doped with an impurity to form P type.

Thus, the steps in the present invention are not anticipated by Kawasaki et al., and the rejection of Claim 4 under 35 USC §102(e) should be withdrawn.

Further, since Claims 6-7, 9, 11 and 13 depend from Claim 4, they are also patentably distinguishable over Kawasaki et al. and

If the Examiner believes that there is any issue which could be resolved by a telephone or personal interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee for such an extension is to be charged to Deposit Account No. 19-3140.

Respectfully submitted,

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APPENDIX I

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 14 was canceled.

The claims were amended as follows:

4. (Twice Amended) A method of making a bottom-gate thin-film transistor comprising:

forming a gate electrode on a substrate;

forming a gate insulating film on the gate electrode;

forming a laminate on said gate insulating film, comprising:

forming a precursor film for an active layer, and

forming a protective insulating film on [the gate insulating] said precursor film without using an etching process, the protective insulating film having a thickness of 100 nm or less;

implanting a dopant [in] when forming one of an LDD region and a source-drain region of the precursor film for the active layer through the protective insulating film without etching said protective insulating film; and

activating the implanted dopant so that a non-doped portion comprises the active layer.

8. (Twice amended) A [The] method of making a bottom-gate thin-film transistor [according to Claim 5] comprising:

forming a gate electrode on a substrate;

forming a gate insulating film on the gate electrode;

forming a laminate comprising a precursor film for an active layer, and a protective insulating film on the gate insulating film, the protective insulating film having a thickness of 100 nm or less;

implanting a dopant in one of an LDD region and a source-drain region of the precursor film for the active layer through the protective insulating film without etching the protective insulating film; and

activating the implanted dopant so that a non-doped portion comprises the active layer;

wherein, in the laminate forming step, an amorphous silicon film is formed on the gate insulating film, the protective insulating film is formed on a surface of the amorphous silicon film by surface oxidation of the amorphous silicon film, and then the amorphous silicon film is crystallized to form the polysilicon film.